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SERVICES FOR SCIENCE AND EDUCATION

VLSI Architecture for Edge Detection of Leaf Images

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ABSTRACT

This paper proposed a new VLSI Architecture for Sobel Edge detector for Cotton and Grape leaf images. This new VLSI Architecture is tested for leaf images using Verilog HDL and Simulated and Synthesized using Xilinx Vivado tool and results shown the low power and low area, utilized less than 0.01% of LUTs and 0.13 w of power only. The same architecture is also extended for Prewitt and Laplace Edge detectors and results shown that utility of power and area is less.

Keywords: Edge Detection, VLSI (Very Large Scale Integration) Architecture, Verilog, LUT (Look Up Table)

INTRODUCTION

Agriculture in India is slowly adapting the advanced technologies, such as Internet of Things (IoT), Artificial Intelligence, Machine Learning, Drones, System on Chips etc. [1]. Image Processing in Agriculture monitors the crop health at each and every stage of farming by providing the required information of crop to identify the plant hazards that effects the good yield. This helps farmers to do farming comfort, Modern and Precision and results the improved quality of production. Processing of agricultural images requires several methods to extract the required information from crop time to time. One such method is Edge Detection.

Edges are defined as the sudden changes of pixel intensities that contains the important information of the scene which is required for image recognition, image segmentation, image retrieval, object detection, object tracking and also for feature extraction. Hence Edge Detection plays a crucial role in computer vision and image processing [2]. Detecting the edges of leaf images will help to identify the various hazards such weeds, poor yield, leaf diseases etc., that differ from crop in shape, texture and corners.

Several research work has been done on Edge Detection in an images. Junfeng Jing [3] given a comprehensive review of edge detection methods starting from hand crafted based to machine learning based. Ahmed Shihab Ahmed [4] given a comparative study and significance of different image processing algorithms like Sobel, Prewitt and canny. They used C programming to execute those algorithms. O. R. Vincent [5] gave a descriptive analysis of Sobel Edge Detection and applied to a 2D spatial images for detecting the edges. Dr. Sumeet Mathur [6] discussed about the Laplacian of Gaussian (LoG) methodology that combines Gaussian filter and Laplace edge detection algorithm to remove noise from the images through edge detection. They implemented this algorithm on X-ray Images but did not mention the software that used.

Huilin Xu [7] proposed a novel edge detection algorithm based on the regularized Laplacian operator by detecting partial differential equations using regularized parameter. Weibin Kong [8] tested Sobel edge detection algorithm with different threshold values and stated that adaptive tresholding gives best results when compared.

All these research focussed on the software processing of edge detection which may be not suitable for real time applications. There is a huge need of research in this field to meet the high-speed computation requirement in real time agriculture applications. This focuses on the growing demand of VLSI (Very Large Scale Integration) as it allows the integration of billions of transistors onto a single chip which can perform multiple operations simultaneously. Edge detection can also be implemented using VLSI for high speed performance and efficiency in agriculture field. In perspective a nominal work is carried [9], [10], [11], [12].

In this paper a new VLSI Architecture is proposed for Sobel Edge Detector. The proposed VLSI Architecture is also applied for Prewitt and Laplace Edge Detectors and tested on leaf images and results are compared. The remaining part of the paper is organised as Section II gives the explanation of Sobel, Prewitt and Laplace Edge Detectors. Section III discuses about the proposed VLSI Architecture for Sobel, Prewitt and Laplace Edge Detection. Section IV shows the results. Section V gives the conclusion and future work to be done.

EDGE DETECTION

Edge detection is one of the important image processing techniques with wide range of applications. Several edge detection algorithms have been developed such as Roberts, Prewitt, Sobel, Laplace, Laplace of Gaussian (LoG), Canny and implemented for Image segmentation and object detection. Here Sobel, Prewitt and Laplace edge detectors are designed and developed VLSI architecture and applied on leaf images of cotton and grape.

Sobel Edge Detection

Sobel Edge Detector works with a mathematical procedure called convolution to calculate the first order derivatives of the images which are also known as the Gradients. It uses two masks or kernels to calculate the gradients in horizontal and vertical directions of an image respectively. These kernels look like

-1	0	+1
-2	0	+2
-1	0	+1

G_x

+1	+2	+1
0	0	0
-1	-2	-1

G_y

Where Gx is the Horizontal kernel that masks over the 3x3 window of the image to get the edges in x-direction and Gy is the vertical kernel that masks over the same 3x3 image to get the edges in ydirection. These two obtained X-direction and y-direction gradients are combined together as shown in equation (1) to get the magnitude of the gradients. This process continues until the kernel masks over the last 3x3 window of the image. The obtained magnitudes are compared with the predefined threshold value to get the exact edge detection of the image.

$$|G| = \sqrt{Gx^2 + Gy^2} \quad (1)$$

Prewitt Edge Detection

Prewitt edge detector works similar to Sobel but with different vertical and horizontal masks or kernels to calculate the gradients in x & y directions. It also uses the same gradient magnitude calculation of Sobel shown in equation (1). Prewitt operator kernels looks like

1	1	1
0	0	0
-1	-1	-1

G_x

-1	0	1
-1	0	1
-1	0	1

G_y

Prewitt operator uses equal weights treating all neighboring pixels equally which results in slight sensitive to noise whereas Sobel uses weighted coefficients that concentrates on pixels closer to center pixel and so better in suppressing the noise. Prewitt has high computational efficiency compared to Sobel. Hence Sobel is used where reduction of noise is preferred and Prewitt is used for computational efficiency

Laplace Edge Detection

Laplace Edge Detector performs the second order derivatives of gradients to detect the rapid changes of intensities/edges. This algorithm is directionally invariant unlike Sobel and Prewitt edge detection algorithms; hence it uses only one Kernel to calculate the gradients in all directions. The Laplace operator kernel looks like

0	-1	0
-1	4	-1
0	-1	0

As the Laplace uses second order derivatives, the presence of noise in the image gets amplified. Hence it is very sensitive to noise. To overcome this, it is often combined with Gaussian smoothing filter together called as Laplacian of Gaussian (LoG). Gaussian smoothing filter reduces the noise in the image and Laplacian operator performs the edge detection which gives the robust detection of edges. Several existing methods used these edge detectors for image segmentation and object detection either by using Matlab/Python. This paper focuses on the VLSI Architecture of Sobel, Prewitt and Laplace Edge Detectors.

PROPOSED ARCHITECTURE

Sobel Edge Detector uses two convolution kernels for detecting the edges of input leaf image in both Horizontal (x) and vertical (Y) directions as shown in equation (1). The convolution operation of input image with both X and Y directions respectively are shown in below equations.

$$Gx = ((p0*Gx0) + (p1*Gx1) + (p2*Gx2) + (p3*Gx3) + (p4*Gx4) + (p5*Gx5) + (p6*Gx6) + (p7*Gx7) + (p8*Gx8)) \quad (2)$$

&

$$Gy = ((p0*Gy0) + (p1*Gy1) + (p2*Gy2) + (p3*Gy3) + (p4*Gy4) + (p5*Gy5) + (p6*Gy6) + (p7*Gy7) + (P8*Gy8)) \quad (3)$$

where p0, p1, p2, p3, p4, p5, p6, p7, p8 are the 9 pixels of 3x3 sliding window of the input leaf image each with 8 bits, accessed from the buffer. Similarly, Gx0, Gx1…., Gx8 are the 9 values of 3x3 Sobel Horizontal kernel for X direction of edges and Gy0, Gy1…., Gy8 are the 3x3 Sobel Vertical Kernels for Y direction of edges. Gx and Gy be the gradients in x & y directions respectively. The Proposed VLSI architecture, to execute these equations (2) & (3), contains a sequence of Array multipliers and Full adders as shown in below figures Fig (1) and Fig (2)

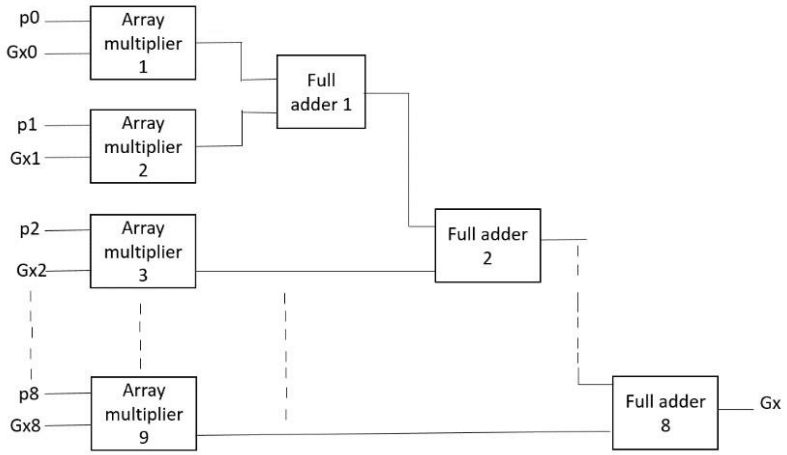

Fig 1: Proposed VLSI architecture to calculate Gx of Sobel Edge Detector

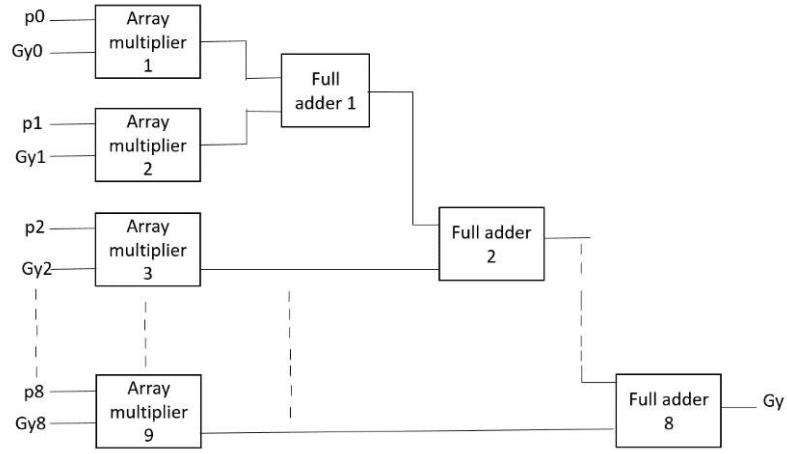

Fig 2: Proposed VLSI architecture to calculate Gy of Sobel Edge Detector

The architecture consists of 9 Array Multipliers and 8 Adders. This operation will continue by 3 x 3 window sliding for the entire input image. Since Sobel has two kernels, the same architecture is used to calculate Gx and Gy.

As the input image consists of pixels of each 8-bits, the values in kernel are also chosen 8 bit, therefor 8x8-bit Array Multipliers are used. The result of product is a 16-bit, the size of Full Adder used is also 16-bit. The architecture of 8x8-bit Array multiplier and a 16-bit Full Adder are shown in Fig 3 and Fig 4 respectively.

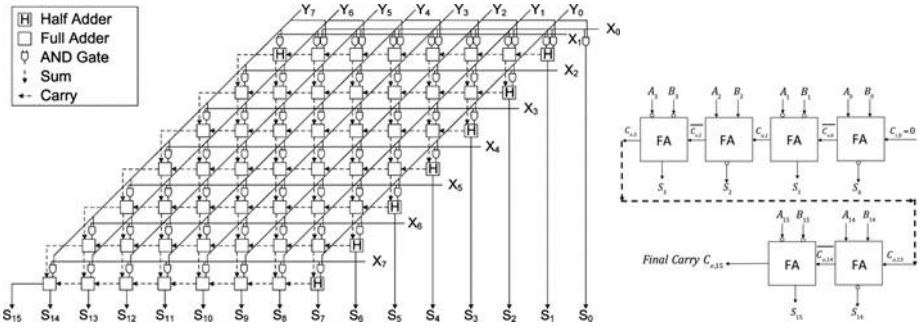

Fig: 3 Architecture of 8-bit Array Multiplier Fig 4: Architecture of 16-bit Full Adder

From Fig 3 the X_0, X_1, ….. , X_7 are 8 bits of each pixel (p0,….,p8) and Y_0, Y_1,…..,Y_7 are the 8-bits of each kernel value (Gx0 to Gx8, Gy0 to Gy8) and the resultant product S_0, S_1, …..S_{15} of 9 product values. This is given as input to the 16, 2- bit Full Adders and such type of 8 Full adders are used for entire architecture and is shown in Fig 4. The Full adder consist of final carry out in addition to the 16 bits therefore the total outputs for Gx and Gy will be of 17-bit values respectively. The obtained Gx and Gy are squared, summed up and then the square root of summation will give the gradient magnitude as shown in equation (1).

The above proposed architecture can also be applied to Prewitt Edge detector as the process of execution of Sobel and Prewitt are same, only the Kernel values are different. Laplace Edge Detector needs only one kernel to detect the edges either Gx or Gy, only one architecture is enough to apply to it.

IMPLEMENTATION AND RESULTS

The proposed VLSI Architectures for Sobel, Prewitt and Laplace Edge detectors are simulated using Verilog HDL in structural model on Xilinx Vivado tool and tested for several images. Out of them two sample images are presented. The first one is a Grape Leaf image with a size of 256x256 and second one is a Cotton leaf image of 256x256 size. These images are first converted into .txt files using Matlab and given as input to Verilog Programming of Proposed VLSI architectures and stored in a buffer. An 18-bit threshold value is selected after multiple iterations for extraction of edges. The code is simulated in Vivado and output is generated in the form of .txt file. The generated output file is converted into image again by using Matlab. The simulated waveforms are shown in figures (5, 6 & 7) and the output images that are converted by Matlab after edge detection are shown in figures (10 & 11).

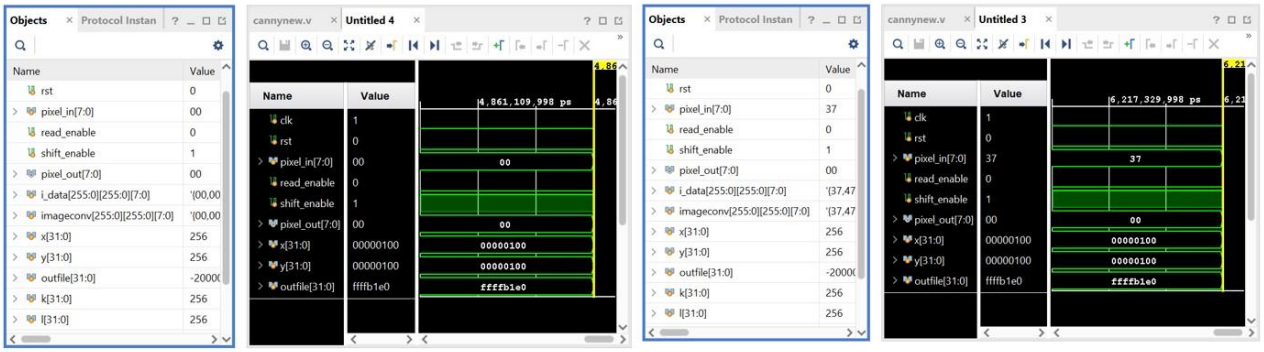

Fig 5: Simulation Waveforms of Sobel Edge Detector for (a) Grape image and (b) Cotton leaf image

Figure 5(a) and 5(b) shows the simulated waveforms for the Proposed VLSI Architecture for Sobel Edge detector when tested on grape leaf and cotton leaf respectively. The both waveforms consists of clk (clock) and rst (reset) inputs to activate the entire process at required times, read_enable and shift_enable are used to read and shift the input data from the .txt file to buffers. Upon on the activation of all signals according to the Verilog code the data from .txt file will store in the i_data register shown in both waveforms. As the input image is 256x256 size the i_data register is chosen to be [0:255] [0:255]. Pixel_in will represent each and every pixel of image with 8-bit width and pixel_out will be the output pixels obtained after edge detection. These pixel_out values are collected and stored in buffer for converting to images. Figures 6 and 7 shows the simulated waveforms of Prewitt and Laplace edge detection respectively.

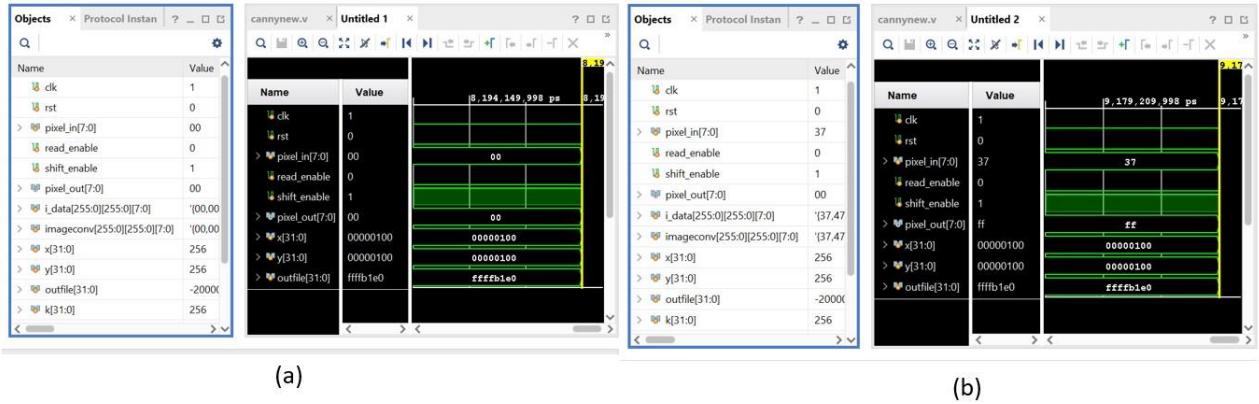

Fig 6: Simulation waveforms of Proposed Prewitt Edge Detector for (a) Grape leaf image (b) Cotton leaf image

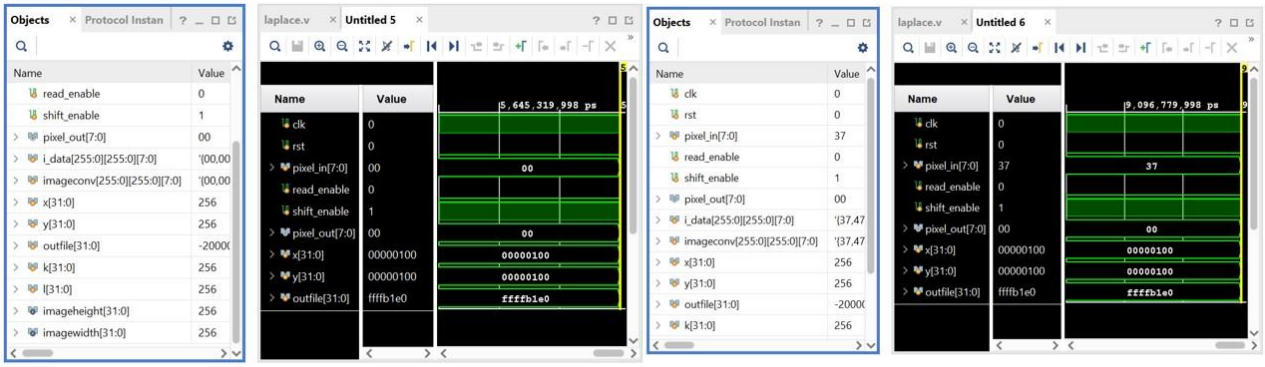

Fig 7: Simulation waveforms of Proposed Laplace Edge Detector for (a) Grape leaf image and (b) Cotton Leaf image

Fig 6(a) shows the waveform of Prewitt Edge detector of grape leaf image and 6(b) shows the waveform for Cotton leaf image. Fig 7(a) shows the waveform of Laplace Edge detector of Grape image and 7(b) shows the waveforms of cotton image. All waveforms consist of same signals as Sobel Edge detection waveforms shown in Fig 5. The RTL (Register Transfer Logic) analysis of Proposed Sobel, Prewitt and Laplace Edge Detector Architectures is shown in Fig 8 & Fig 9.

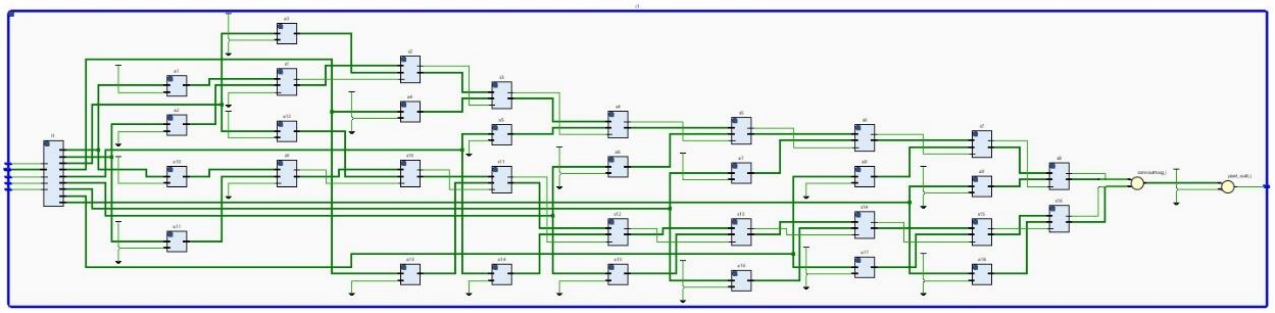

Fig 8: RTL Analysis of Proposed Sobel and Prewitt Edge Detector

The RTL analysis will be same for Sobel and Prewitt Edge detectors as both shares same architecture for edge detection as shown in Fig (8). But the Laplace edge detector contains only one kernel for edges in all directions, it only uses half architecture of Sobel/Prewitt Edge Detection. The RTL Analysis of Laplace Edge Detector is shown in below Fig (9).

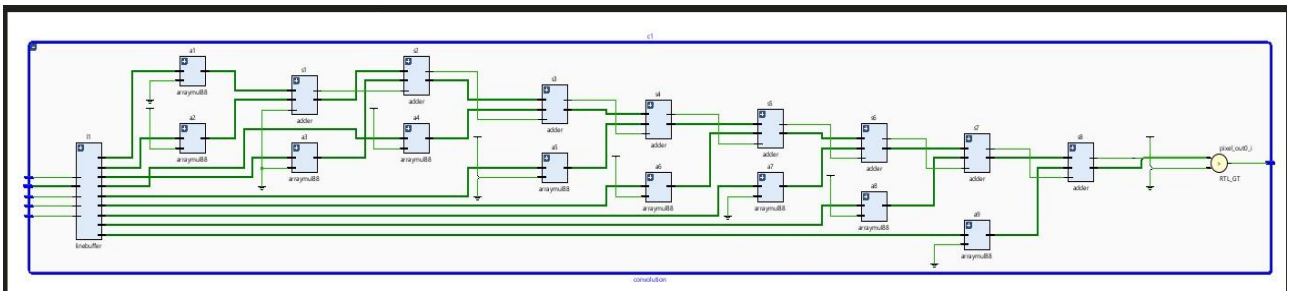

Fig 9: RTL Analysis of Proposed Laplace Edge Detector

The input images, Grape Leaf and Cotton Leaf that are given as inputs to test the Proposed architectures and the output edge detected images are shown in below figures Fig 10 & 11. Fig 10 shows the original input image of Grape Leaf and its Sobel, Prewitt and Laplace Edge Detected outputs. Fig 11 shows the original input image of cotton Leaf and its Sobel, Prewitt and Laplace edge detected outputs.

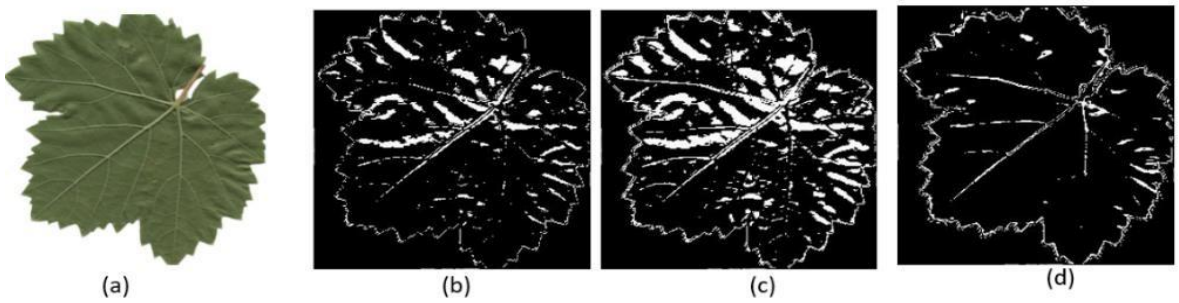

Fig 10: (a) Original input image of Grape leaf with 256x256 size, (b) Edge Detected output of Proposed Sobel Architecture, (c) Edge deetcted output of Proposed Prewitt Architecture, (d)Edge Detected output of Proposed Sobel Architecture.

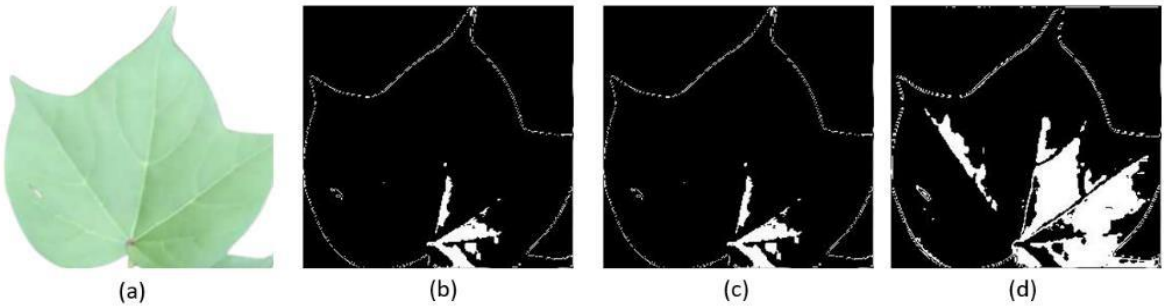

Fig 11: (a) original input image of Cotton leaf with 256x256 size, (b) Edge Detected output of Proposed Sobel Architecture, (c) Edge Detected output of Proposed Prewitt Architecture, (d) Edge Detected output of proposed Laplace Architecture

After simulation, the Proposed VLSI Architectures are synthesized and implememted on Zedboard of xc7z020clg484-1 family. Table 1 shows the effective utilization of LUTs (Look Up Tables), inputoutput (IO) ports after implementation on zedboard. The proposed VLSI architecture of Sobel Edge Detector uses only 0.01% of LUTs and only 0.13 w of power is consumed. As Prewitt Edge detector is designed with same architecture, same uitlization values are obatined for prewitt edge detetcion algorithm where as Laplace Edge Detector uses less than 0.01% of LUTs and 0.13w of power.

Table 1: Utilization of LUTs

Resource	Available		Utilized		Utilization %		
		Proposed Sobel	Proposed Prewitt	Proposed Laplace	Proposed Sobel	Proposed Prewitt	Proposed Laplace
LUT	53200	1	1	<1	0.01	0.01	<0.01
DSP	22	0	0	0	0.00	0.00	0.00

IO	200	8	8	8	4.00	4.00	4.00

CONCLUSION

The Proposed VLSI Architecture well designed for Sobel Edge detector is simulated and synthesized using Verilog HDL and Vivado tool. The proposed architecture also got sucessful application for Prewitt and Laplace Edge Detectors. This new VLSI architecture uses only 0.01% of LUTs for Sobel and Prewitt algorithm and less than 0.01% Utilization of LUTs for Laplace Edge Detector when implemented on Zedboard of xc7z020clg484-1 family. This proposed architecture uses only 0.13 w of on-chip power for all the three Eedge Detectors. The new architetcure is tested for several leaf images and observed the required detection of edges that contains the information. These edges can be further used for segmentation and can also be used as features for classification of crop and weeds and other hazards that effects good yield and results in qualtiy production by making Agriculture Precision. As a future work VLSI Architecture for Classification based on the detected edges will be designed with less hardware complexity and less power consumption.

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