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Electrical Properties of Sub-1nm Diameter Silicon Nanowire Metal-Oxide-Semiconductor Device

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ABSTRACT

In this short communication, the electrical properties of a 0.7nm diameter Silicon nanowire metal-oxide-semiconductor device are theoretically calculated. The properties are: Intrinsic Fermi energy level in Si of the Silicon nanowire, conduction band offset at the oxide/Si interface, Fowler-Nordheim electron tunneling onset field, oxide leakage current density at the FN onset field, electrical breakdown field for a 10^{-4} A/cm^2 oxide current density, electron and hole channel mobility, and total oxide/Si interface trap densities. It is considered that the SiNW MOSFET is the ultimate transistor for complementary MOS technology in Silicon.

Keywords: MOS device, SiO_2, Silicon Nanowire, Total interface trap density, Carrier mobility.

SHORT COMMUNICATION

A Silicon nanowire (SiNW) Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) is considered for the Silicon technology after the current FinFET and nanoribbon FET Gate-All-Around (GAA) technology with gate area scaling. Increasing the effective gate area provides better electrostatic gate control and lowers leakage currents in the GAA FETs. An ab initio quantum transport simulation study is discussed by S. Liu et al. The discussion promises the viability of 3nm to 5nm gate length SiNW FET having a 1nm diameter nanowire channel in the GAA FET [1]. The experiments with quantum interference transistor having a Zn-Porphyrin molecule as a sub-3nm gate length limits the frequency of operation to 7 KHz due to gate switching time delay, when THz frequency of operation is the demand [2]. Also, the DC current across a Benzene-1, 4-dithiolate molecule is theoretically found to be about 100 to 200 μA at about 2V across the electrodes [3]. These are some of the alternative attempts of finding a better future device technology. A recently published article by the author has presented the electrical properties of a 1nm diameter SiNW MOS device that is convincingly practical and feasible, having larger than 3nm gate lengths [4]. The present brief communication reduces the diameter to 0.7nm when the bandgap of the hydrogen terminated Silicon in the SiNW becomes 3.5 eV [5]. Here, the electrical properties of the SiNW MOS device are calculated again. The longitudinal electron effective mass reduces with the increased diameter and increases with the reduced diameter. It is taken as 0.49m for one conduction valley in the longitudinal [100] direction of the SiNW [5]. It is to be noted that the gate oxide in the GAA FETs is atomic layer deposited (ALD) SiO_2 which is nearly as good as the thermal SiO_2, although ALD oxides are under research also.

For the 0.7nm SiNW having a bandgap of Silicon in the SiNW as 3.5 eV as E, and the electron effective mass in the [100] longitudinal direction of the electric field for one conduction valley

as 0.49m as dm/m, the intrinsic Fermi energy level E_i below the silicon conduction band (CB) is calculated as E_i = dE = 0.49 x 3.5 = 1.715 eV. This calculation utilizes the universal mass-energy equivalence relation of dE/E = dm/m, where the bandgap energy of Si is E and the free electron mass is m. dE and dm are differential energy and mass of the electron in the materials Silicon and Silicon dioxide [6-9]. For Silicon dm/m is taken as 0.49 and for SiO_2 it is taken as 0.42 [10-11]. Given that the aligned E_i with that in Si for the SiO_2 as a dielectric is 3.75 eV, the CB offset at the oxide/Si interface is calculated to be 3.75 – 1.715 = 2.035 eV. Also, with the minimum electric field for electron heating in the oxide to be 2 MV/ (cm-eV) [6], the Fowler-Nordheim (FN) electron tunnelling onset field for the nanowire MOS device will be 4.07 MV/cm. The theoretical FN slope constant is calculated to be B as 128.5 MV/cm where the electron effective mass in SiO_2 is 0.42m and the CB offset is 2.035 eV [6-7]. The leakage current density in the oxide at the FN onset electric field of 4.07 MV/cm can be calculated using the formula for the FN electron tunnelling current density at 300K temperature to be 5.8 x 10^{-7} A/cm^2. The electrical breakdown field for an oxide leakage current density of 1.76 x 10^{-4} A/cm^2 is calculated to be 4.9 MV/cm. The above calculated electrical properties show that this device is also practically feasible and the author feels confident that the SiNW diameter can be reduced to 0.7nm. The confined Silicon in the SiNW is just another parabolic semiconductor with a wider bandgap of 2.5 to 3.5 eV, and all the electrical properties of the MOS device can be calculated theoretically as above as for a MOS device on any other parabolic semiconductor [8]. The average electron and hole mobility in the channel of the transistors will range from 30 to 300 cm^2/V-s as described earlier [4]. It needs to be mentioned that knowing the bandgap of Silicon and the longitudinal electron effective mass in the SiNW is more important than the diameter of the SiNW. Silicon in the 1nm or a 0.7nm diameter SiNW becomes a direct bandgap semiconductor. Silicon photonics is therefore possible such as its use as an optical waveguide. The confinement of light though is very small and deters the possibility of integrating optics. Also, increased temperature up to 400K may degrade the device performance. Presently, Biosensing and gas sensing are applications of a SiNW FET.

CONCLUSION

A 0.7nm diameter SiNW MOS device having Gate-All-Around is practical after studying the electrical properties of the MOS device as above at 300K temperature, given that experimental challenges exist.

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